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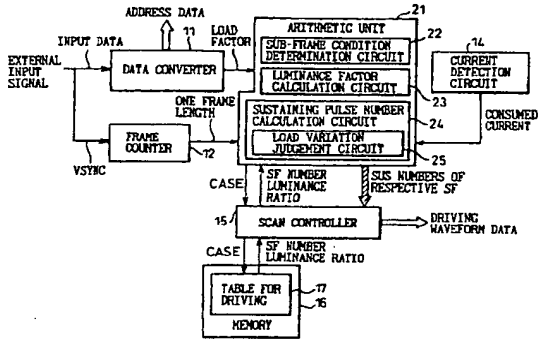
(54) Plasma display unit

(57) A frame time-sharing type plasma display unit, in which a display frame for one screen is constituted by a plurality of sub-frames, and in which the luminance of the respective sub-frames is determined by a sustaining pulse number, comprises: a frame length calculation circuit (12) for calculating the length of one frame from the length of one cycle of a vertical synchronization signal; a sub-frame condition determination circuit (22) for determining from the length of one frame the number of sub-frames, the luminance of the sub-frame and a total sustaining pulse number; a load factor calculation circuit (11) for calculating a load factor, which is a ratio of a number of display cells that are illuminated to a total number of display cells, from an external input signal; a luminance factor calculation circuit (23) for determining a maximum display luminance from the consumed power and calculating a luminance factor; and a sustaining pulse number calculation circuit (24) for correcting the luminance drop due to load from the total sustaining pulse number, the luminance ratio and the load factor for the respective sub-frame and calculating sustaining pulse numbers for the respective sub-frames. The use of a luminance table is thereby avoided.

Fig.6



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Description

[0001] The present invention relates to a display unit (hereinafter, referred to as a plasma display unit (PDP unit)) using a plasma display panel (hereinafter, referred to as a PDP), and more particularly to a plasma display unit for displaying gradation by making the display luminescence time different by weighting every sub-frame.

[0002] In recent years, in display units, there have been growing demands for thinner units, increases of varieties of information to be displayed and installation conditions, larger screens and better resolution, and display units are required which can meet these demands. PDP units are display units which can handle these demands. In the PDP units, when displaying gradation, in general, a display frame is constituted by a plurality of sub-frames, the respective sub-frame periods are weighted so that they are differentiated, and the respective bits of gradation data are displayed by the corresponding sub-frames.

[0003] The PDP has a memory effect, and each cell is set for a state conforming to the display data. Luminescence for display (display luminescence) is effected by application of an AC voltage. As will be described later, this display luminescence intensity is varied by the number of the cells which are illuminated, and there is a problem in that the luminance ratio between the sub-frames deviates. In addition, consumed current and power also vary in accordance with the number of the cells which are illuminated. It is desirable to solve the problem entailed by the variation in display.

[0004] Regarding PDP types, there are two-electrode type PDPs in which selected discharge (address discharge) and maintained discharge (discharge for display luminescence) are carried out with two electrodes and a three-electrode type PDP in which a third electrode is used to carry out address discharge. Three-electrode type PDP units are disclosed in Japanese Unexamined Patent Publication (Kokai) Nos. 7-140928 and 9-185343, and therefore, a detailed description thereof will be omitted here and only the basic construction and operation thereof will be briefly described below.

[0005] Fig. 1 of the accompanying drawings shows the basic construction of the three-electrode type PDP units. As shown therein, connected to a plasma display panel (PDP) 1 are an address driver 2 for outputting a signal to be applied to an address electrode, a Y scan driver 3 for outputting a signal to be applied to a scan electrode (Y electrode), an X common driver 4 for outputting a signal to be applied to a common sustaining discharge electrode (X electrode), and a Y common driver 5 for outputting a sustaining discharge signal to be applied to the Y electrode via the Y scan driver 3. A control circuit 6 has a display data control part 7 for generating from a display data inputted from the outside a display data signal to be outputted to the address driver 2 and a panel driving control part 8 for outputting a signal other than the display data which is related to the driving of the panel. The panel driving control part 8 has a scan driver control part 9 for generating a control signal which is related to a scan to be outputted to the Y scan driver 3 and a common driver control part 10 for generating a control signal related to the sustaining discharge.

[0006] Fig. 2 of the accompanying drawings shows a frame construction for carrying out a 32-gradation display.

[0007] A gradation display in the PDP unit is generally carried out by making each bit of the display data correspond to the sub-frame time and changing the length of the sub-frame period in accordance with the weighting of the bits. For instance, when the 32-gradation display is carried out, the display data is represented by five bits, the display of one frame is constituted by five sub-frames SF1 to SF5, and the display of the respective bit data is carried out within the respective sub-frame periods. In reality, in order to control timings, there are provided rest periods when no operation is performed.

[0008] The respective sub-frames SF1 to SF5 are constituted by a reset period when all display cells of the panel are put in a uniform state, an addressing period when wall electric charges corresponding to display data are accumulated in display cells, and a sustaining period when a discharge for display is carried out by the display cells in which wall electric charges are accumulated by applying a sustaining discharge signal. As shown in Fig. 2, the lengths of the reset period and the addressing period are the same over the respective sub-frames, but the sustaining period is different. The lengths of the reset period and the address period of the respective sub-frames are identical. As described above, when the 32-gradation display is carried out, in general, the ratio between the lengths of the sustaining discharge periods becomes 1:2:4:8:16. The differences in luminance of 32 gradations from 0 to 31 can be displayed by selecting a combination of sub-frames to be illuminated in each display cell.

[0009] Fig. 3 of the accompanying drawings is a block diagram showing a schematic construction of a part related to the control circuit 6. Of the external input signals, the display data inputted into a data converter 11 and a vertical synchronization signal (VSYNC) is inputted into a frame counter 12. The display data that is supplied from the outside generally takes a format in which gradation data of respective pixels are continuous, and they cannot be converted into the format of the sub-frames as they are. Then, to cope with this, the data converter 11 temporarily stores the display data in the frame memory and then converts it into a format for the address data to be outputted to the address driver 2. Furthermore, the data converter calculates for a load factor, which will be described later.

[0010] The frame counter 12 detects the length of

one frame (frame length) from the vertical synchronization signal. There are various types of signals that are inputted from the outside, and it is generally true that PDP units are designed to deal with those signals by changing the control timing based on the frame length detected by the frame counter 12. The number of sub-frames (SF number) and the luminance ratio thereof are stored in a driving table 17 for a memory (ROM) 16 in accordance with the frame length. An arithmetic unit 13 calculates an address CASE of the memory 16 in which corresponding information is stored based on the frame length, applies the CASE so calculated on the memory 16 via a scan controller 15 and determines a SF number and a luminance ratio corresponding to the frame length.

[0011] The arithmetic unit 13 decreases a time required for the reset period and the addressing period from the SF number, calculates a sustaining discharge period in one frame and calculates a total sustaining pulse number for one frame from the sustaining discharge period and one predetermined sustaining pulse cycle. Sustaining pulse numbers of the respective sub-frames are stored in a luminance table 19 of a memory (ROM) 18 in accordance with the total sustaining pulse number and the luminance ratio. The arithmetic unit 13 calculates from the total sustaining pulse number an address MCB of the memory 18 in which corresponding information is stored, applies the address MCB so calculated together with the luminance ratio on the memory 18 and determines sustaining pulse numbers for the respective sub-frames. Conventionally, the sustaining numbers of the respective sub-frames are determined for control. Fig. 4 shows an example of the luminance table 19.

[0012] Next, the load factor and the consumed power will be described. The effective brightness of the display by the respective sub-frames is determined by the luminance and period of the sustaining discharge. The sustaining discharge periods of the respective sub-frames have a predetermined ratio (luminance ratio) and, if the number (display load) of display cells that are illuminated at the respective sub-frames is identical, the luminance by the sustaining discharge becomes identical, and the brightness of display has a predetermined ratio which is identical to the ratio of the sustaining discharge period. However, the currents supplied to the X electrode and Y electrode become different in response to the number of display cells which are illuminated simultaneously, and when current values are different, there is caused a voltage drop, due to distribution resistance, this resulting in a different luminescence intensity (luminance) even if sustaining discharges are identical. Specifically speaking, if there are a number of display cells to be illuminated, in other words, when the load factor is large, the luminance becomes low, while if there are few display cells to be illuminated, in other words, when the load factor is small, the luminance becomes high. Due to this, when the load factor becomes different among the respective sub-frames, there is caused a difference between a luminance ratio that is actually obtained and a preset luminance ratio, the gradation which is displayed by a combination of the sub-frames cannot be displayed accurately, and in a worse case, there is caused a problem that there occurs an inversion in brightness between gradations.

[0013] With a view to solving the aforesaid problem, in the above-described invention disclosed in Japanese Unexamined Patent (Kokai) Publication No. 9-185343, a plurality of sustaining pulse numbers, that will result in a predetermined luminance, are stored for the respective sub-frames in accordance with the load factors, and the sustaining pulse number is determined by the sustaining pulse numbers in accordance with the load factors calculated by the data converter 11, whereby the luminance ratios of the respective sub-frames are maintained constant irrespective of load factors.

[0014] The large power consumption by the PDP unit is related to sustaining discharge. As described above, the currents supplied to the X electrode and Y electrode during a sustaining discharge depend on the number of display cells that are illuminated. Therefore, a value is related to the consumed power which is obtained by multiplying the load factors of the respective sub-frames by the length of sustaining discharge period thereof. In the PDP unit, the upper limit is provided for the consumed power (current), and a display is required which is as bright as possible within the range. To cope with this, the consumed power is detected, and if the consumed power does not exceed the upper limit, the total sustaining pulse number is increased to as high as possible within the range. Due to this, for example, if the display is bright, although the number of display cells that are illuminated is increased, the total sustaining pulse number is decreased, and therefore the consumed power falls within the range. On the contrary, if the display is not bright, the number of display cells that are illuminated is decreased and therefore the total sustaining pulse number is increased. Thus, the actual display does not become too dark, and the decrease in consumed power is not large. Even with a display like this, no feeling of physical disorder is felt by all user.

[0015] A current detection circuit 14 shown in Fig. 3 is a circuit for detecting current flowing into the unit, and the consumed power is calculated from the detected current and the consumed power so calculated is then outputted to the arithmetic unit 13. The arithmetic unit 13 corrects the sustaining pulse numbers of the respective sub-frames read out of the luminance table 19 in accordance with the consumed power and outputs corrected sustaining pulse numbers for the respective sub-frames to the scan controller 15. The scan controller 15 outputs signals for controlling the X common driver 4 and Y common driver 5 such that sustaining discharge can be carried out the number of times corresponding to the corrected sustaining pulse number during the sustaining discharge period for the respective sub-frames.

[0016] As described above, the consumed power depends on the number of display cells that are illuminated. Therefore, the consumed power corresponds to a weighted mean value resulting from average weighting of the load factors of the respective sub-frames depending on the length of the sustaining discharge period thereof. Consequently, instead of detecting current directly flowing into the unit, a weighted mean value resulting from average weighting of the load factors of the respective sub-frames depending on the length of the sustaining discharge period thereof is sometimes calculated for estimation of the consumed power, and the above-mentioned correction is carried out based on the estimated consumed power.

[0017] As shown in Fig. 3, the relationship between the total sustaining pulse number and the sustaining pulse numbers of the respective sub-frames is stored in advance in the luminance table 19 of the memory 18, and the aforesaid correction in response to the consumed power is carried out for the sustaining pulse numbers of the respective sub-frames read out of the luminance table 19. This causes a problem that a large-scale memory (ROM) is required in order to prepare an accurate luminance table.

[0018] In addition, the values stored in the luminance table 19 are, as shown in Fig. 4 of the accompanying drawings, positive integers, and values below the decimal point are rounded to the nearest whole number. Due to this, stored values include round-off errors. When the aforesaid correction is carried out for the sustaining pulse number, there is caused a problem that the error is increased and the predetermined luminance cannot be obtained. Of course, it is possible to conceive of expanding the capacity of the memory 18 so as to make the luminance table 19 more accurate, but in this case, too, there occurs a problem that a memory 18 of large capacity has to be used.

[0019] In addition, in the conventional PDP unit, the load factors of the respective sub-frames are calculated for each frame so as to determine corresponding sustaining pulse numbers for the respective sub-frames. In addition, corrections are carried out by the consumed power, and the sustaining discharge is controlled with the corrected sustaining pulse numbers so obtained. Due to this, there is caused a problem that the sustaining pulse numbers of the respective sub-frames vary for each frame and this causing flickering.

[0020] Fig. 5 of the accompanying drawings is a graph showing variations in the load factor during display. As shown in the Figure, small variations in load factor are found in ranges surrounded by a dotted line. For a variation into the different range, it is needless to say that corrections are needed in accordance with the luminance ratio and consumed power of the sub-frame but, in the conventional PDP unit, corrections were carried out even in the ranges surrounded by the dotted line, and this caused flickering.

[0021] Accordingly, it is desirable to realize a PDP unit which does not need a memory for storing a luminance table so as to simplify the construction thereof, which can perform more accurate operations so as to improve the display quality and can provide a stable display without flickering.

[0022] According to a plasma display unit embodying the present invention, the sustaining pulse numbers of respective sub-frames are determined through an operation using a total sustaining pulse number, a luminance ratio, a load factor and the consumed power rather than using a luminance table.

[0023] In other words, there is provided a frame time-sharing type plasma display unit in which a display frame for one screen is constituted by a plurality of sub-frames, and in which the luminance of the respective sub-frames is determined by a sustaining pulse number, the plasma display unit comprising a frame length calculation circuit for calculating the length of one frame from the length of one cycle of a vertical synchronization signal, a sub-frame condition determination circuit for determining, from the length of one frame, the number of sub-frames, the luminance of the sub-frame and a total sustaining pulse number, a load factor calculation circuit for calculating a load factor, which is a ratio of a number of display cells that are illuminated to a total number of display cells, from an external input signal, a luminance factor calculation circuit for determining a maximum display luminance from the consumed power and calculating a luminance factor and a sustaining pulse number calculation circuit for correcting the luminance drop due to load from the total sustaining pulse number, the luminance ratio and the load factor for the respective sub-frame and operating sustaining pulse numbers for the respective sub-frames.

[0024] Thus, in an embodiment of the present invention, the luminance table can be removed and the influence of round-off errors can be reduced.

[0025] Reference will now be made, by way of example, to the accompanying drawings, in which:

Fig. 1 (described above) is a block diagram showing the construction of a PDP (plasma display panel) unit,

Fig. 2 (described above) is a diagram showing the construction of sub-frames for gradation display in the PDP unit,

Fig. 3 (described above) is a diagram showing the schematic construction of a control circuit of a conventional PDP unit,

Fig. 4 (described above) is a diagram showing a luminance table for use in the conventional example,

Fig. 5 (described above) is a graph showing variations in load factor,

Fig. 6 is a diagram showing the construction of a control circuit of a PDP unit according to an embodiment of the present invention,

Fig. 7 is a flow chart showing a calculating process

of sustaining pulse numbers for the respective sub-frames in the embodiment,

Fig. 8 is a flow chart showing an calculating process of a luminance factor β,

Fig. 9 is a flow chart showing a modified example of the calculating process of the luminance factor β,

Fig. 10 is a flow chart showing another modified example of calculating process of the luminance factor β, and

Fig. 11 is a flow chart showing another modified example of the calculating process of the luminance factor β.

[0026] A PDP unit embodying the present invention has a construction such as shown in Fig. 1, and is different from a conventional unit only in part of a control circuit 6.

[0027] Fig. 6 is a block diagram showing the schematic construction of the control circuit 6 according to the embodiment of the present invention, and this Figure corresponds to Fig. 3. As is clear when compared with Fig. 3, the control circuit 6 of the embodiment is different from the conventional example in that the memory 18 storing the luminance table 19 is removed and that sustaining pulse numbers of respective sub-frames are calculated by an arithmetic unit 21. The arithmetic unit 21 includes a sub-frame condition determination circuit 22, a luminance factor calculation circuit 22 and a sustaining pulse number calculation circuit 24. The subframe condition determination circuit 22 performs substantially the same processes as those done in the prior art. The circuits in the arithmetic unit 21 are realized by hardware or software.

[0028] The luminance factor calculation circuit 23 comprises a consumed power calculating circuit for calculating the estimated consumed power from the load factor to thereby determine a maximum display luminance in accordance with the consumed power and calculate a luminance factor. In this case, the load factor calculating circuit calculates the load factor for the respective sub-frames and the arithmetic unit 21 comprises a weighted mean load factor calculating circuit for calculating the weighted mean load factor from the load factors and luminance ratios for the respective subframes, the weighted mean load factor being regarded as the load factor.

[0029] The sustaining pulse number calculation circuit 24 comprises a load factor memory for storing load factors, and a load factor variation calculating circuit 25 for calculating a difference between the calculated load factor and the load factor of the previous frame stored in the load factor memory, wherein when the difference does not exceed a predetermined threshold value, the sustaining pulse numbers of the respective sub-frames are not calculated and the sustaining pulse numbers of respective sub-frames in a previous frame are outputted as sustaining pulse numbers for the sub-frames of the current frame, while the difference exceeds the predetermined threshold value, calculated sustaining pulse numbers for the respective sub-frames are outputted.

[0030] With this construction, in a case where the variation in load factor is small, since the sustaining pulse numbers of the respective sub-frames do not change, a stable display free from flickers can thus be provided.

[0031] The luminance factor calculation circuit 23 does not estimate the consumed power from the load factor as described above, but comprises a consumed power calculation circuit for detecting the consumed power of the unit and calculating the consumed power from a value so detected and a comparison circuit for comparing the consumed power with a preset reference power, wherein when the consumed power exceeds the reference power, the luminance factor is decreased, while the consumed power does not exceed the reference power, the luminance factor is increased.

[0032] In this case, too, it may be constructed such that when the variation is small as with the previous case, the sustaining pulse numbers are maintained, and only when the variation is large, the previous sustaining pulse numbers are revised to the corrected sustaining pulse numbers.

[0033] Fig. 7 is a flow chart showing calculation and correction processes of the sustaining pulse numbers of the respective sub-frames carried out by the control circuit 6. Referring to Fig. 7, the processes performed by the control circuit 6 will be described below.

[0034] In Step 101, as with the conventional example, a frame counter 12 detects the length of one frame (frame length) Tv from a vertical synchronization signal. In Step 102, the subframe condition determination circuit 22 of the arithmetic unit 21 calculates based on the frame length Tv an address CASE of a memory 16 in which corresponding information is stored, applies a CASE so calculated on the memory 16 via a scan controller 15 and determines an SF number (SFNUM) corresponding to the frame length Tv stored in a driving table 17 and luminance ratios (WSFi) of the respective sub-frames.

[0035] In Step 103, the subframe condition determination circuit 22 of the arithmetic unit 21 calculates a time DVT=SFNUM×(RT+AT) required by other than a sustaining discharge period (luminance display period) from SFNUM and times required for driving the PDP such as preset reset period (RT) and address period (AT). A time ST=Tv- DVT for use for the sustaining discharge period is calculated from a difference between Tv and DVT. Furthermore, a total sustaining pulse number NSUSmax=ST/SPT is calculated from one sustaining pulse cycle SPT which is preset.

[0036] In Step 104, reads in load factors Dli of the respective sub-frames calculated by data converter 11 is read. In Step 105, the arithmetic unit 21 calculates a weighted mean load factor $MWDL(t)=\Sigma(Dli\times WSFi)/\Sigma WSFi$ from the load factors Dli and the luminance ratios WSfi of the respective sub-

frames. The weighted mean load factors so calculated are then stored.

[0037] In Step 106, the luminance factor calculation circuit 23 calculates a β process as shown in Fig. 8. In Step 201, an estimated consumed power Pw is calculated from the weighted mean load factor MWDL(t). According to the specific operating method, for instance, the relationship between the load factor and the consumed power is investigated in advance, an equation for calculating the consumed power from the load factor is stored in the arithmetic unit, and a calculation is carried out in accordance with the calculating equation so stored. In the simplest method, a product of power per unit load and the weighted mean load factor MWDL(t) is calculated. In Step 202, a luminance factor $\beta=Pt/Pw$ is calculated which is a ratio with a preset reference power Pt.

[0038] In Step 107, the sustaining pulse number calculation circuit 24 calculates a load variation value $\Delta DL=MWDL(t)-MWDL(t-1)$ from a difference between the weighted mean load factor MWDL(t-1) existing when the sustaining pulse numbers were set before storage and the MWDL(t) currently calculated. In Step 108, an absolute value of ΔDL and a preset threshold value ΔDLth are compared. The calculation and comparison in the Steps 107 and 108 are carried out by the load variation judgement circuit 25 in the sustaining pulse number calculation circuit 24.

[0039] In a case where the absolute value ΔDL is small, in Step 109, the sustaining pulse numbers CSPi(t-1) of the respective sub-frames of the previous frame are regarded as the sustaining pulse numbers CSPi(t) of the respective sub-frames of the current frame. In a case where the absolute value ΔDL is large, in Step 110, a correction coefficient $\gamma i=MWDL(t)/DLi$ is calculated from the calculated weighted mean load factor MWDL(t) and the load factor Dli.

[0040] In Step 111, the sustaining pulse numbers $CSPi(t)=\gamma i\times NSUSmax\times\beta\times(WSFi/\Sigma WSFi)$ are calculated from the correction coefficient γi, total sustaining pulse number NSUSmax, luminance ratio WSFi, luminance factor β. In Step 112, a weighted mean load factor MWDL(t-1) to be used in operation for the following frame is replaced with MWDL(t) currently calculated.

[0041] In Step 113, the sustaining pulse numbers CSPi(t) calculated as described above are outputted.

[0042] Through the processes described above, when the load factors change moderately or they vary slightly, the luminance of the sub-frames does not change and flickering can be reduced. For example, in a case where the screen is scrolled within the same scene, normally, since ΔDL<2%, if ΔDLth=3%, the change in luminance resulting from correction can be suppressed within the same scene.

[0043] Moreover, the luminance table 19 used in the conventional construction is no longer used, and therefore the memory can be omitted. In addition, since the influence from the round-off errors can be reduced, the variation in luminance is reduced, thereby making it possible to improve the display quality.

[0044] In the β process performed in Step 106 above, the variation in load factor was judged using the consumed power Pw estimated from the weighted mean load factor MWDL(t), but it is possible to use the consumed power Pi that is calculated from the consumed power detected by the current detection circuit 14 in Fig. 6. Moreover, it is desirable to use both the consumed power Pw estimated from the weighted mean load factor MWDL(t) and the consumed power Pi that is calculated from the consumed power detected by the current detection circuit 14 and correct them thereafter.

[0045] Fig. 9 is a flow chart showing such a modified example to the β process.

[0046] In Steps 201 and 202, as with the embodiment described above, Pw and β are calculated. In Step 203, an actual consumed power Pi is calculated from the consumed power detected by the current detection circuit 14 for the display of the previous frame. In Step 204, the calculated consumed power Pi is compared with the preset reference power Pt. If Pi is larger, in step 205, the luminance β factor is decreased, and on the contrary, if Pi is smaller, in Step 206, the luminance β factor is increased. If Pi=Pt , β is outputted as it is.

[0047] Fig. 10 is a flow chart showing another modified example to the β process.

[0048] The processes in Steps 201 to 203 are identical to those shown in Fig. 9. In Step 211, a difference ΔP=Pi- Pt between the actual consumed power Pi and the preset reference power Pt is calculated. In Step 212, ΔP is compared with a preset threshold value ΔPth, and if ΔP is larger, in Step 213, the luminance β factor is decreased, and on the contrary, if ΔP is smaller, in Step 214, ΔP is further compared with -ΔPth, and if ΔP is smaller, the luminance β factor is increased in Step 215, and if ΔP is smaller, β is maintained as it is. By using the luminance factor β thus obtained, when the consumed power varies slightly, the luminance factor does not change, and therefore, flickering can be reduced.

[0049] Fig. 11 is a further modified example of the β process. The power supply for the unit is buffered by a capacitor or the like, and, for example, in a case where the consumed power alternately repeats an increase and a decrease every frame, according to the process shown in Fig. 10, the luminance factor β varies every frame, and flickering cannot be reduced. With a process in Fig. 11, however, such a problem can be solved.

[0050] The processes in Steps 201 to 203 and 211 are identical to those in Fig. 10. In Step 221, an integrated value is calculated by adding ΔPS calculated in the current frame to an integrated value of a difference ΔPS between Pi for the frames upto the previous one and Pt. In Step 222, ΔPS is compared with a preset threshold value ΔPSth, and if ΔPS is larger, in Step 223, the luminance β factor is decreased, and if ΔPS is smaller, in Step 224, ΔPS is further compared with -

ΔPth, and if ΔPS is smaller, the luminance β factor is increased in Step 225, and if ΔPS is smaller, β is maintained as it is. After Steps 223 and 225, ΔPS is reset in Step 226. Through these processes ΔPS is averaged in a plurality of frames, and only when the averaged one is larger, is the luminance β factor changed. With these processes, even when the consumed power is repeatedly increased and decreased, there no flickering is generated.

[0051] As has been described heretofore, according to an embodiment of the present invention, irrespective of variation in display load as a whole or in the respective sub-frames, a PDP unit can be realized in which a display of optimum brightness can be effected without deterioration in gradation display.

Claims

1. A frame-time sharing type plasma display unit in which a display frame for one screen is constituted by a plurality of sub-frames, and in which the luminance of said respective sub-frames is determined by a sustaining pulse number, said plasma display unit comprising;

   a frame length calculation circuit for calculating the length of one frame from the length of one cycle of a vertical synchronization signal,
   a sub-frame condition determination circuit for determining the number of sub-frames, the luminance of said sub-frame and a total sustaining pulse number from the length of said one frame,
   a load factor calculation circuit for calculating a load factor, which is a ratio of a number of display cells that are illuminated to a total number of display cells, from an external input signal,
   a luminance factor calculation circuit for determining a maximum display luminance from the consumed power and calculating a luminance factor and
   a sustaining pulse number calculation circuit for correcting the luminance drop due to load from said total sustaining pulse number, said luminance ratio and said load factor for said respective sub-frame and calculating sustaining pulse numbers for said respective sub-frames.

2. A plasma display unit as set forth in claim 1, wherein said luminance factor calculation circuit comprises a consumed power calculating circuit for calculating said consumed power estimated from said load factor for determining said maximum display luminance in accordance with said consumed power and calculating said luminance factor.

3. A plasma display unit as set forth in claim 2, further comprises a weighted mean load factor calculating circuit for calculating a weighted mean load factor from said load factors and said luminance ratios for said respective sub-frames, said weighted mean load factor being outputted as the load factor.

4. A plasma display unit as set forth in any one of claims 1 to 3, wherein

   said sustaining pulse number calculation circuit comprises a load factor memory for storing said load factors, and a load factor variation calculating circuit for calculating a difference between said calculated load factor and a load factor stored in said load factor memory, wherein
   when said difference does not exceed a predetermined threshold value, the sustaining pulse numbers of said respective sub-frames are not calculated and the sustaining pulse numbers of respective sub-frames in a previous frame are outputted as sustaining pulse numbers for the sub-frames of the current frame and,
   when said difference exceeds the predetermined threshold value, the calculated sustaining pulse numbers for the respective sub-frames are outputted.

5. A plasma display unit as set forth in claim 1, wherein said luminance factor calculation circuit comprises,

   a consumed power calculation circuit for detecting a consumed power of the unit and calculating said consumed power from a value so detected, and
   a comparison circuit for comparing said consumed power with a preset reference power, wherein
   when said consumed power exceeds said reference power, said luminance factor is decreased and, when said consumed power does not exceed said reference power, said luminance factor is increased.

Fig.1

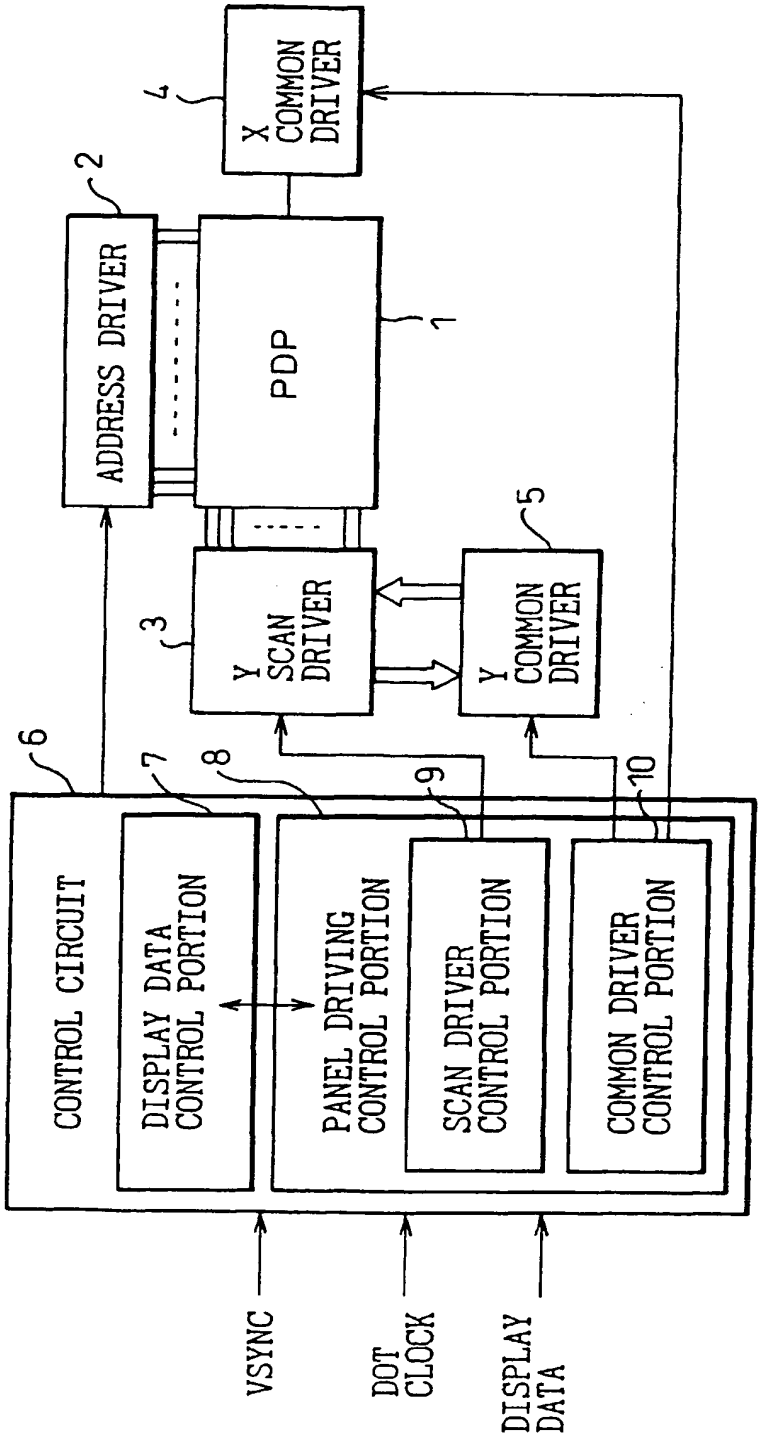

X COMMON DRIVER
4
ADDRESS DRIVER
2
PDP
1
Y SCAN DRIVER
3
Y COMMON DRIVER
5
6
7
8
9
10
CONTROL CIRCUIT
DISPLAY DATA CONTROL PORTION
PANEL DRIVING CONTROL PORTION
SCAN DRIVER CONTROL PORTION
COMMON DRIVER CONTROL PORTION
VSYNC
DOT CLOCK
DISPLAY DATA

Fig.2

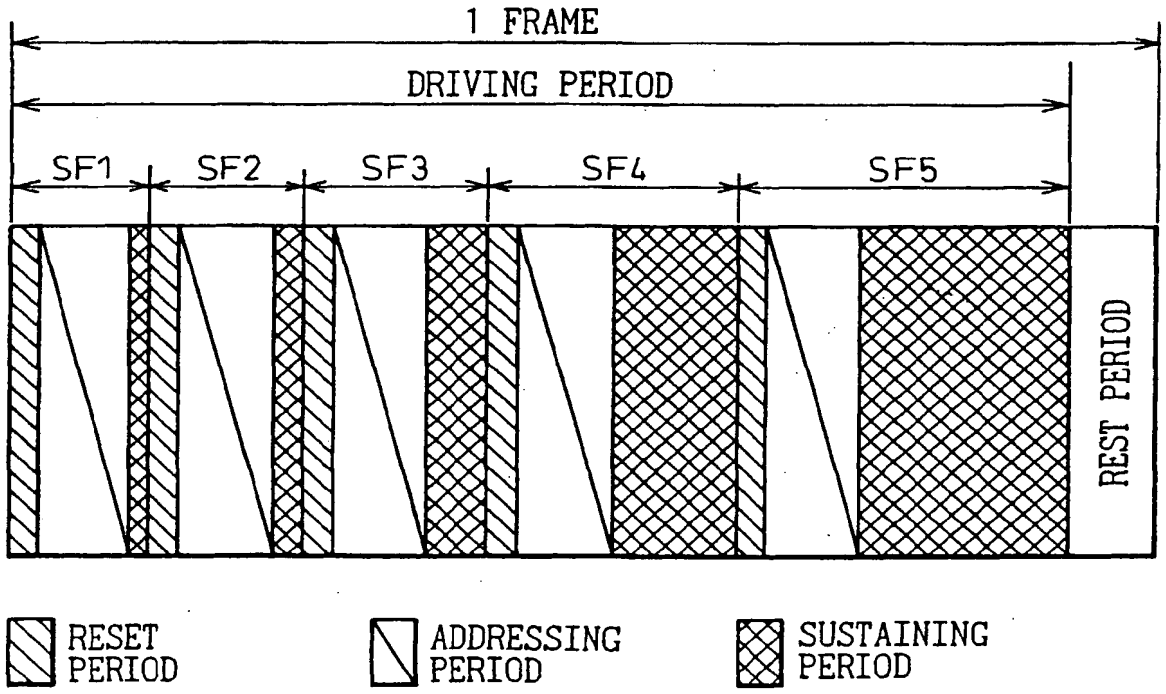

1 FRAME
DRIVING PERIOD
SF1
SF2
SF3
SF4
SF5
REST PERIOD
RESET PERIOD
ADDRESSING PERIOD
SUSTAINING PERIOD

Fig.3

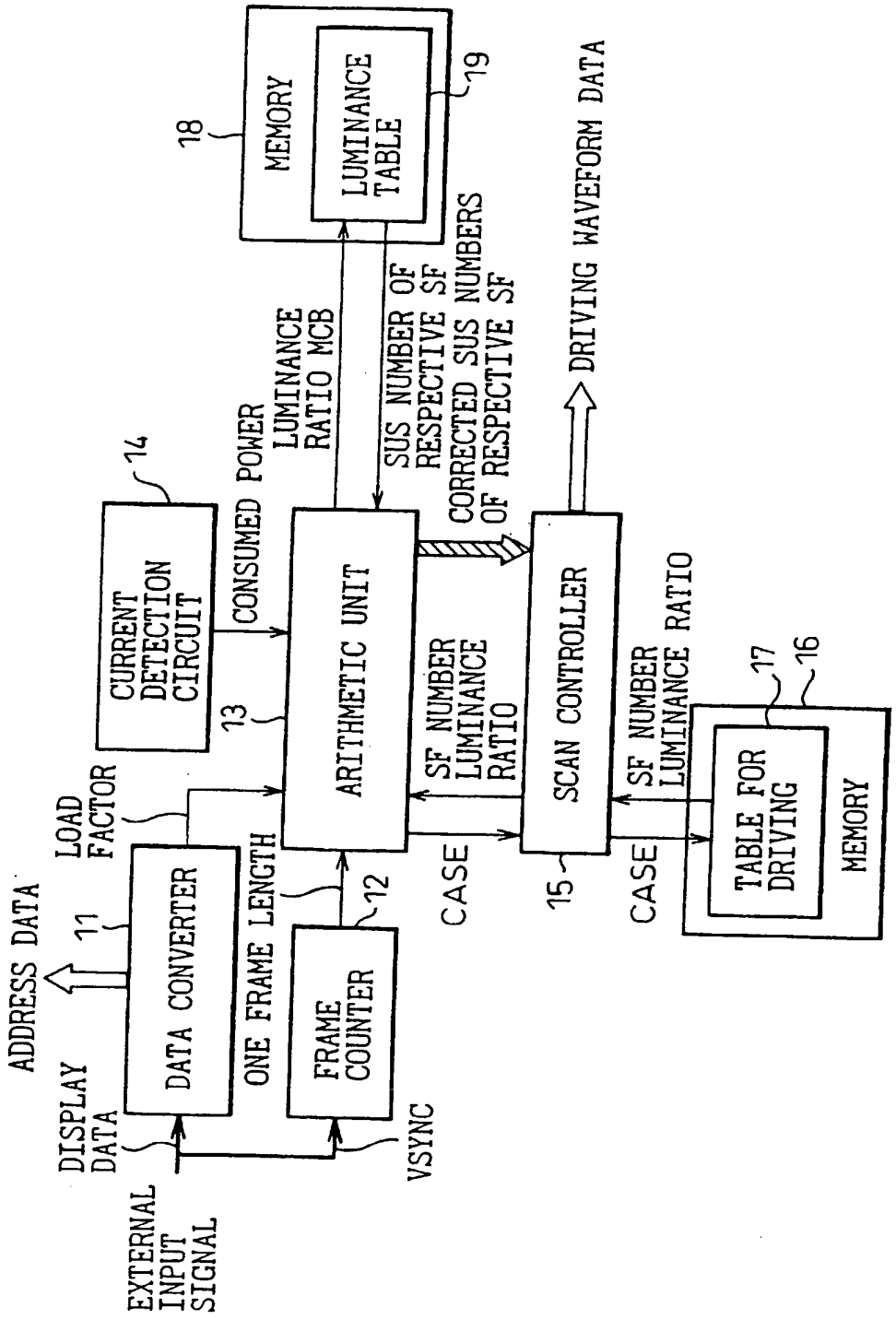

EXTERNAL INPUT SIGNAL
DISPLAY DATA
ADDRESS DATA
11
DATA CONVERTER
LOAD FACTOR
ONE FRAME LENGTH
FRAME COUNTER
12
VSYNC
14
CURRENT DETECTION CIRCUIT
CONSUMED POWER
13
ARITHMETIC UNIT
18
MEMORY
LUMINANCE TABLE
19
LUMINANCE RATIO MCB
SUS NUMBER OF RESPECTIVE SF
CORRECTED SUS NUMBERS OF RESPECTIVE SF
SF NUMBER LUMINANCE RATIO
CASE
15
SCAN CONTROLLER
DRIVING WAVEFORM DATA
SF NUMBER LUMINANCE RATIO
CASE
17
16
TABLE FOR DRIVING
MEMORY

Fig.4

TOTAL SUSTAINING PULSE NUMBER	SUSTAINING PULSE NUMBERS OF RESPECTIVE SF				
	SF1	SF2	SF3	SF4	SF5
31	1	2	4	8	16
93	3	6	12	24	48
158	5	11	21	40	81
248	8	16	32	64	128
312	10	21	40	81	160

Fig.5

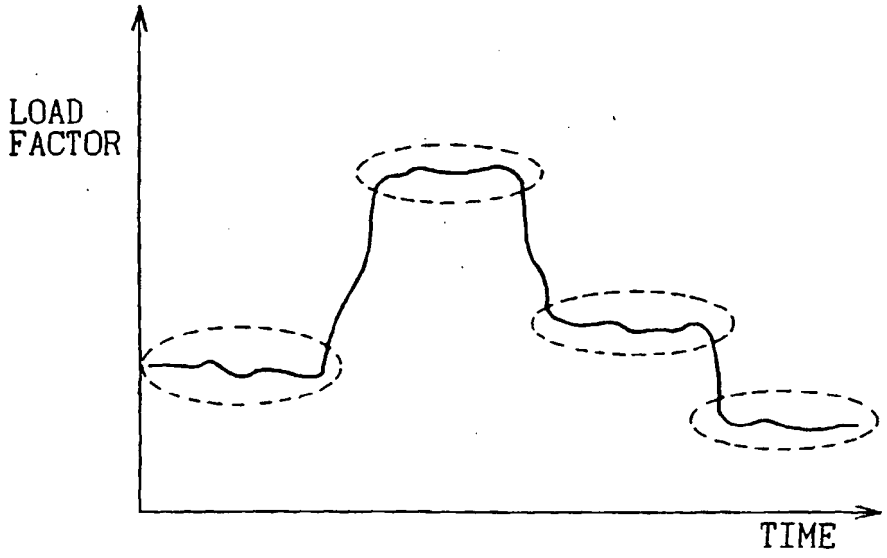


Fig.6

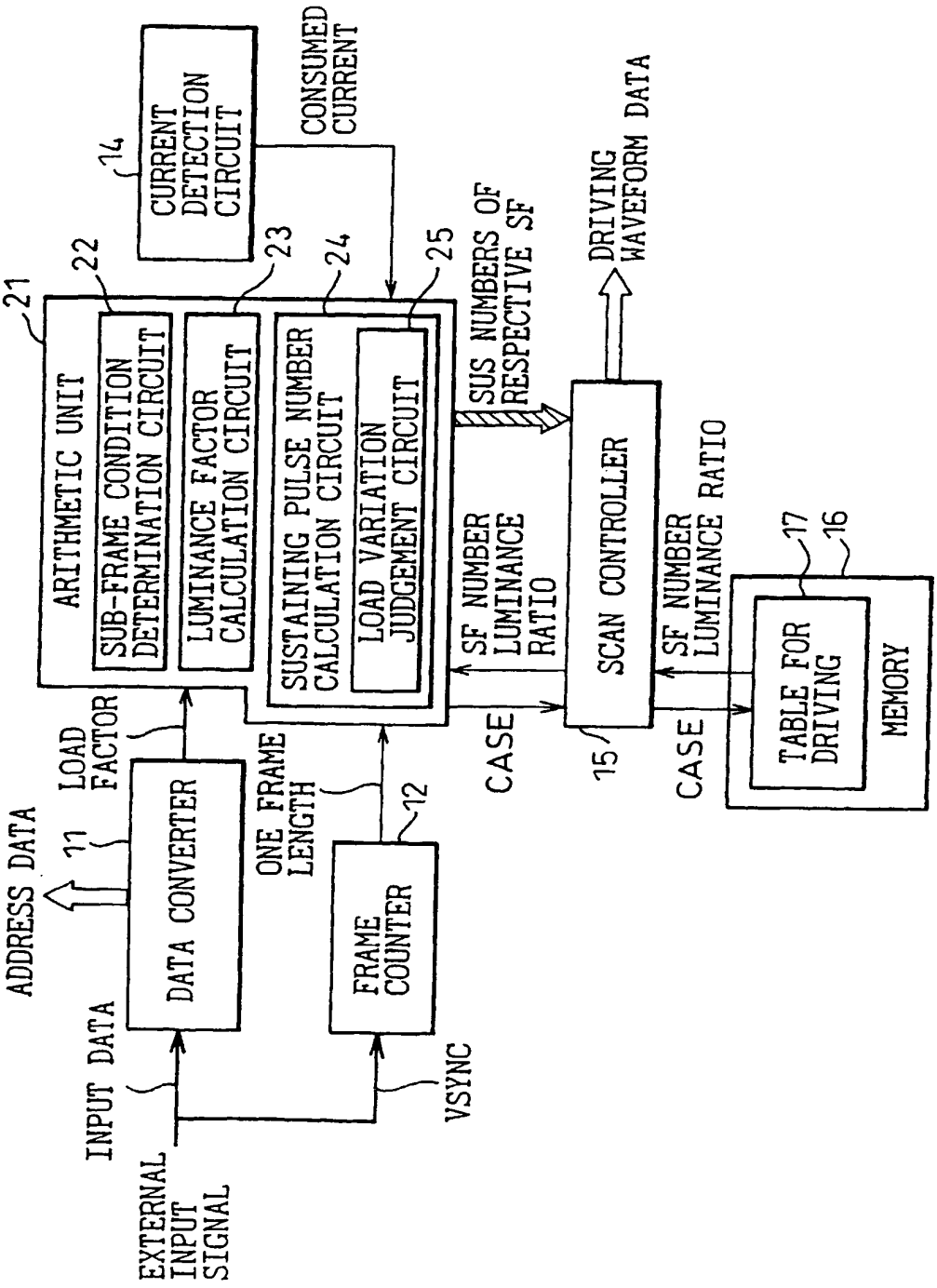

EXTERNAL INPUT SIGNAL
INPUT DATA
ADDRESS DATA
11
DATA CONVERTER
LOAD FACTOR
ONE FRAME LENGTH
12
FRAME COUNTER
VSYNC
21
ARITHMETIC UNIT
22
SUB-FRAME CONDITION DETERMINATION CIRCUIT
23
LUMINANCE FACTOR CALCULATION CIRCUIT
24
SUSTAINING PULSE NUMBER CALCULATION CIRCUIT
25
LOAD VARIATION JUDGEMENT CIRCUIT
14
CURRENT DETECTION CIRCUIT
CONSUMED CURRENT
SUS NUMBERS OF RESPECTIVE SF
SF NUMBER LUMINANCE RATIO
CASE
15
SCAN CONTROLLER
DRIVING WAVEFORM DATA
SF NUMBER LUMINANCE RATIO
CASE
17
16
TABLE FOR DRIVING
MEMORY

Fig.7

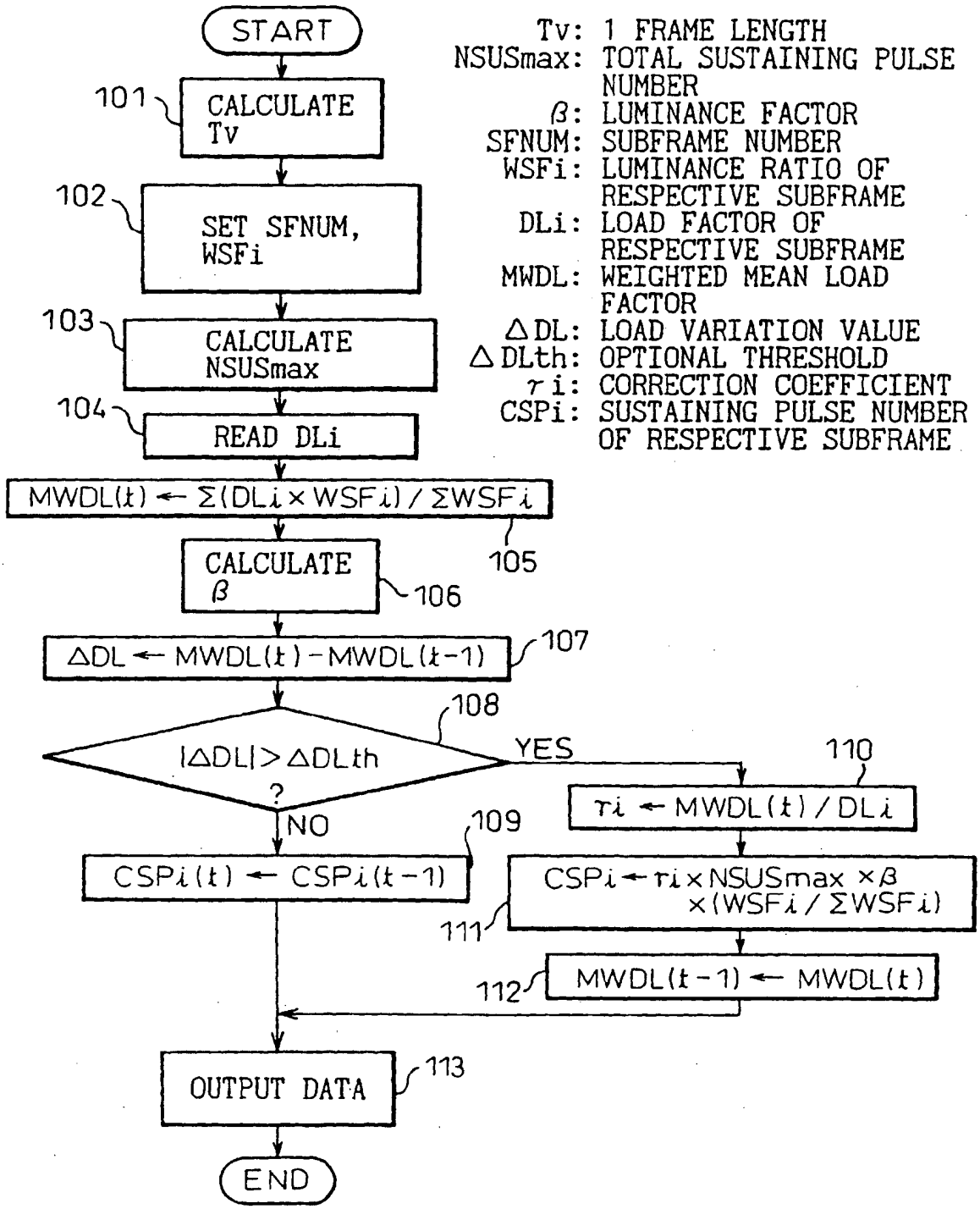

START
101
CALCULATE Tv
102
SET SFNUM, WSFi
103
CALCULATE NSUSmax
104
READ DLi
MWDL(t) ← Σ(DLi × WSFi) / ΣWSFi
105
CALCULATE β
106
ΔDL ← MWDL(t) - MWDL(t-1)
107
108
|ΔDL| > ΔDLth ?
YES
NO
110
τi ← MWDL(t) / DLi
109
CSPi(t) ← CSPi(t-1)
CSPi ← τi × NSUSmax × β × (WSFi / ΣWSFi)
111
112
MWDL(t-1) ← MWDL(t)
OUTPUT DATA
113
END
Tv: 1 FRAME LENGTH
NSUSmax: TOTAL SUSTAINING PULSE NUMBER
β: LUMINANCE FACTOR
SFNUM: SUBFRAME NUMBER
WSFi: LUMINANCE RATIO OF RESPECTIVE SUBFRAME
DLi: LOAD FACTOR OF RESPECTIVE SUBFRAME
MWDL: WEIGHTED MEAN LOAD FACTOR
ΔDL: LOAD VARIATION VALUE
ΔDLth: OPTIONAL THRESHOLD
τi: CORRECTION COEFFICIENT
CSPi: SUSTAINING PULSE NUMBER OF RESPECTIVE SUBFRAME

Fig.8

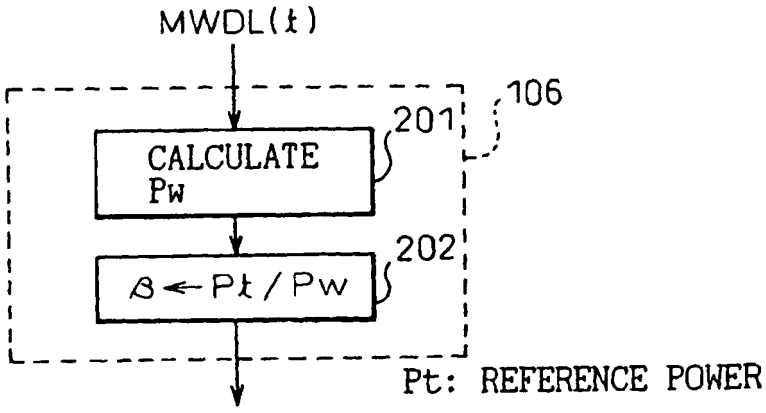

MWDL(t)
106
201
CALCULATE
Pw
202
β ← Pt / Pw
Pt: REFERENCE POWER

Fig.9

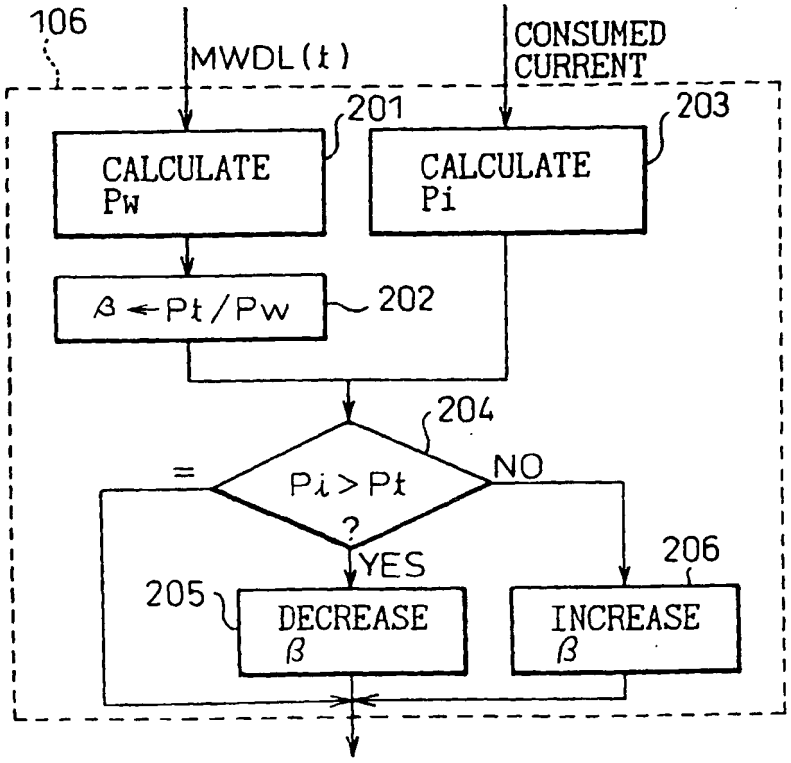

106
MWDL(t)
CONSUMED
CURRENT
201
CALCULATE
Pw
203
CALCULATE
Pi
β ← Pt / Pw
202
204
Pi > Pt
?
=
NO
YES
205
DECREASE
β
206
INCREASE
β

Fig.10

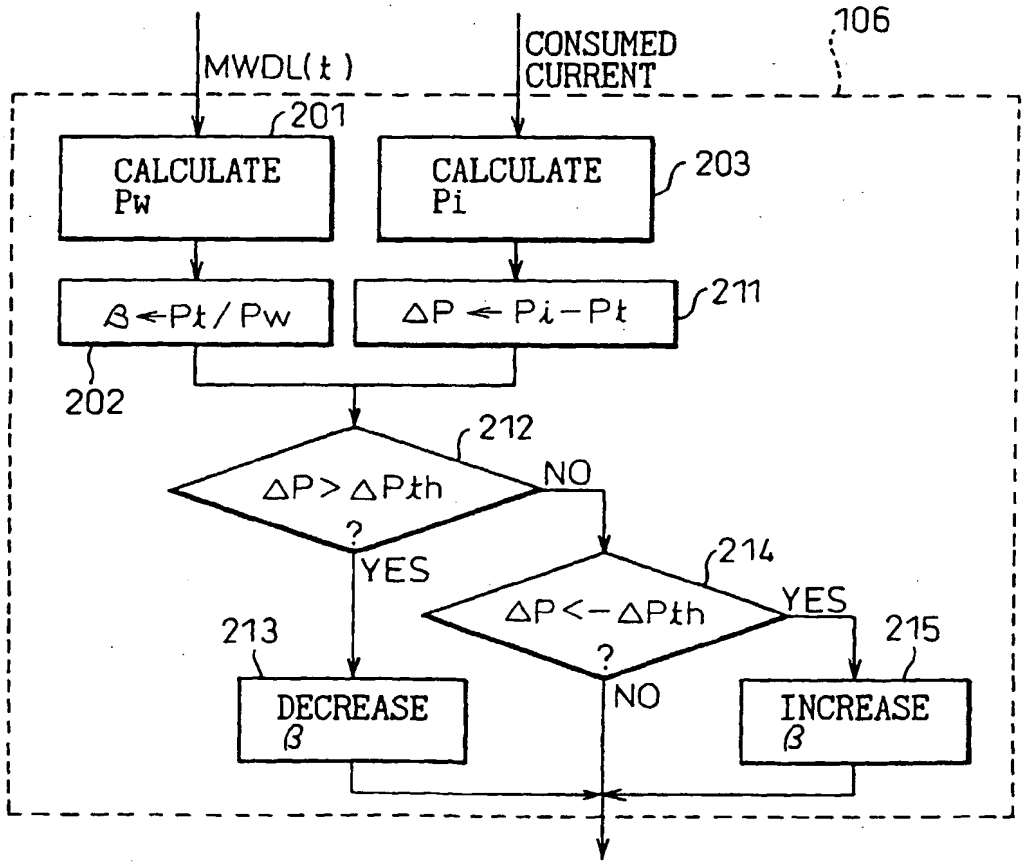
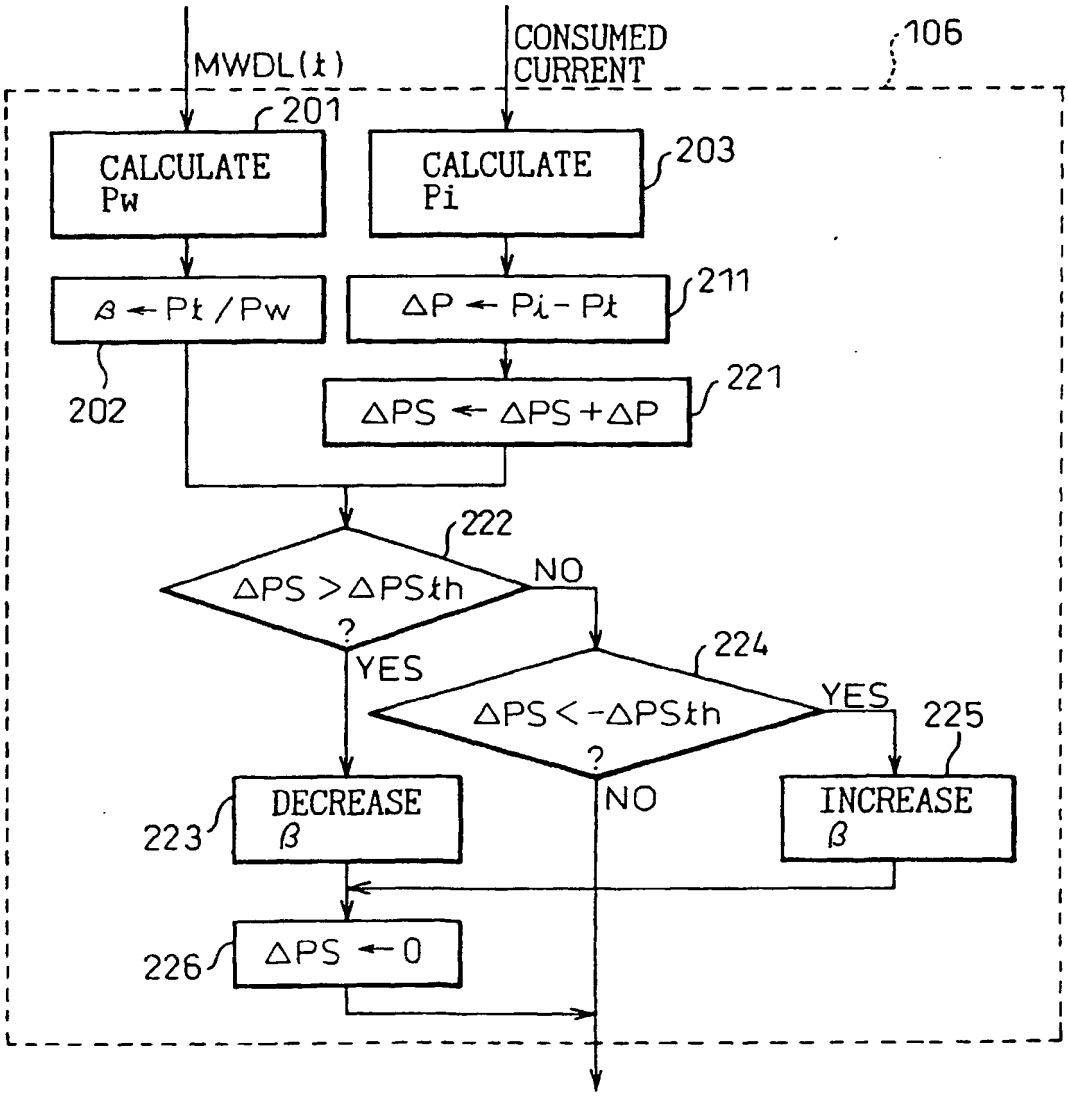

MWDL(t)
CONSUMED CURRENT
106
201
CALCULATE Pw
CALCULATE Pi
203
β←Pt/Pw
ΔP←Pi−Pt
211
202
212
ΔP>ΔPth ?
NO
YES
214
ΔP<−ΔPth ?
YES
213
215
NO
DECREASE β
INCREASE β

Fig.11


MWDL(t)
CONSUMED CURRENT
106
201
CALCULATE Pw
CALCULATE Pi
203
β ← Pt / Pw
ΔP ← Pi - Pt
211
202
ΔPS ← ΔPS + ΔP
221
222
ΔPS > ΔPSth ?
NO
YES
224
ΔPS < -ΔPSth ?
YES
225
NO
DECREASE β
INCREASE β
223
226
ΔPS ← 0

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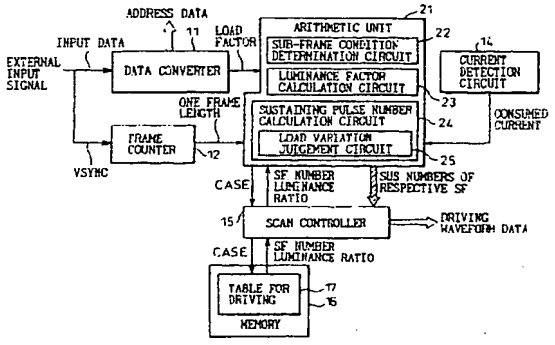
(54) Plasma display unit

(57) A frame time-sharing type plasma display unit, in which a display frame for one screen is constituted by a plurality of sub-frames, and in which the luminance of the respective sub-frames is determined by a sustaining pulse number, comprises: a frame length calculation circuit (12) for calculating the length of one frame from the length of one cycle of a vertical synchronization signal; a sub-frame condition determination circuit (22) for determining from the length of one frame the number of sub-frames, the luminance of the sub-frame and a total sustaining pulse number; a load factor calculation circuit (11) for calculating a load factor, which is a ratio of a number of display cells that are illuminated to a total number of display cells, from an external input signal; a luminance factor calculation circuit (23) for determining a maximum display luminance from the consumed power and calculating a luminance factor; and a sustaining pulse number calculation circuit (24) for correcting the luminance drop due to load from the total sustaining pulse number, the luminance ratio and the load factor for the respective sub-frame and calculating sustaining pulse numbers for the respective sub-frames. The use of a luminance table is thereby avoided.

Fig.6



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Application Number
EP 00 30 2725

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A,D	EP 0 653 740 A (FUJITSU LTD) 17 May 1995 (1995-05-17) * abstract * * page 3, line 1 - line 56 * * page 7, line 53 - page 9, line 21 * * page 10, line 3 - line 25; figures 7-11 *	1-5	
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
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